

S.no	NOS	Question	Option 1	Option 2	Option 3	Option 4	Correct Answer	Difficulty level	Marks
1	ELE/N1427.Developing Functional Design for SOC Modules	What is the primary output document of the functional design phase for a System-on-Chip (SOC) module?	Gate-Level Netlist	Functional Design Specification (FDS)	Bill of Materials (BoM)	Foundry Process Manual	B	Easy	8
2	ELE/N1427.Developing Functional Design for SOC Modules	Which language is typically used to create a high-level behavioral model of an SOC module before Register-Transfer Level (RTL) coding begins?	Assembly Language	C++ with TLM (Transaction-Level Modeling)	Verilog or VHDL	Python	B	Easy	7
3	ELE/N1427.Developing Functional Design for SOC Modules	The practice of dividing an SOC into smaller, well-defined blocks with clear interfaces is known as:	Testbench Generation	Modular Partitioning	Physical Synthesis	Static Timing Analysis (STA)	B	Easy	7
4	ELE/N1427.Developing Functional Design for SOC Modules	What is the main purpose of defining a Test Plan during the functional design phase of an SOC module?	To calculate the chip's final area.	To determine the manufacturing cost.	To specify the verification strategy and coverage goals.	To select the fabrication process technology.	C	Medium	9
5	ELE/N1427.Developing Functional Design for SOC Modules	Which critical concept ensures that different functional blocks within an SOC can communicate reliably by synchronizing their data transfer?	Power Gating	Clock Skew	Interface Protocol Definition	Pin Multiplexing	C	Medium	9
6	ELE/N1428.Coordinating and Implementing SOC Design Verification and Testin	Which modern verification methodology primarily uses constrained random test cases and functional coverage metrics to ensure design robustness?	Gate-Level Simulation	Static Timing Analysis (STA)	Universal Verification Methodology (UVM)	Design Rule Checking (DRC)	C	Easy	5
7	ELE/N1428.Coordinating and Implementing SOC Design Verification and Testin	What is the main objective of Formal Verification in SOC design?	To check timing constraints.	To generate a test netlist.	To mathematically prove or disprove the functional	To estimate power consumption.	C	Easy	5
8	ELE/N1428.Coordinating and Implementing SOC Design Verification and Testin	A Testbench for an SOC module is best defined as:	The physical circuit board used for manufacturing.	The final production environment for the chip.	The simulation environment that applies stimuli and	The documentation of design features.	C	Easy	5
9	ELE/N1428.Coordinating and Implementing SOC Design Verification and Testin	What is the purpose of Functional Coverage in a verification plan?	To track the physical area utilization of the chip.	To measure which specified design features or	To calculate the time taken to run the simulation.	To monitor the number of design errors found.	B	Medium	7
10	ELE/N1428.Coordinating and Implementing SOC Design Verification and Testin	Which critical component within the UVM verification environment is responsible for generating the constrained random stimuli applied to the Design Under Test (DUT)?	Monitor	Checker	Scoreboard	Sequencer	D	Hard	9
11	ELE/N1428.Coordinating and Implementing SOC Design Verification and Testin	The process of executing a Test Program on a manufactured silicon device to identify physical defects (e.g., shorts, opens) is known as:	Functional Simulation	Formal Analysis	Post-Silicon Validation/Testing	Synthesis	C	Hard	9
12	DGT/VSQ/N0102.Employability Skills	Which behavior demonstrates Professionalism when a technical problem causes a project delay?	Blaming the component supplier.	Ignoring the issue and continuing work.	Notifying the manager immediately and proposing a corrective	Asking a colleague to solve it without supervision.	C	Easy	2
13	DGT/VSQ/N0102.Employability Skills	In a team meeting, the primary benefit of practicing active listening is:	To wait for your turn to speak.	To take minimal notes quickly.	To fully understand the speaker's technical input and	To judge the speaker's presentation style.	C	Easy	2
14	DGT/VSQ/N0102.Employability Skills	What is the immediate and most crucial action to take upon discovering an electrical hazard (e.g., exposed wire) in the VLSI lab?	Attempt to fix it yourself immediately.	Take a picture of the hazard for documentation.	Report it to the supervisor and/or designated safety	Inform only the co-worker nearest to the hazard.	C	Medium	3
15	DGT/VSQ/N0102.Employability Skills	Why is awareness of Intellectual Property Rights (IPR) important for a VLSI Design Engineer?	To ensure all team members get equal salary.	To ensure the company's chip designs and proprietary	To avoid sharing your work on social media.	To speed up the fabrication process.	B	Medium	3
16	DGT/VSQ/N0102.Employability Skills	Which non-verbal signal is a key indicator of confidence and respect during a professional presentation or discussion?	Speaking very loudly.	Avoiding eye contact with the audience.	Maintaining good eye contact and confident body	Talking continuously without pausing.	C	Hard	5

17	DGT/VSQ/N0102. Employability Skills	The annual assessment process that formally evaluates an employee's work performance, skills, and adherence to professional standards is called a/an:	Request for Proposal (RFP)	Bill of Materials (BoM)	Performance Appraisal	Client Contract Review	C	Hard	5
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